What is claimed is:

1. A method of forming a dual damascene interconnect in an integrated circuit comprising:

providing a substrate having a first etched region therein;

filling said first etched region with a protective layer;

coating said protective layer with a resist layer;

patterning said resist layer and said protective layer to define an opening encompassing said first etched opening wherein said protective layer is recessed within said first etched opening;

thereafter forming a second etched region encompassing a top portion of said first etched region;

thereafter removing said resist layer and said protective layer; and

thereafter filling said first and second etched regions with a conductive material to complete formation of said interconnect.

2. The method according to Claim 1 wherein said protective material is a bottom antireflective coating (BARC) material.

3. The method according to Claim 2 wherein said BARC material has the following properties:

it absorbs light at a wavelength used to expose said resist;

it completely fills said first etched region; and

it can be partially removed by a developer used to remove said resist.

4. The method according to Claim 2 wherein said BARC material comprises polyimide or organic type ARC material.

5. The method according to Claim 1 wherein said first etched region forms a via hole and wherein said second etched region forms a trench and wherein said via hole and said trench together form a dual damascene opening.

6. The method according to claim 1 wherein the said protective layer recessed within said first etched region has a height of between about 50% and 95% of a height of said first etched region.

7. The method according to Claim 1 wherein said first and second etched region are etched through an insulating layer comprising silicon dioxide or low dielectric constant dielectric materials.

8. The method according to Claim 7 further comprising depositing a hard mask layer overlying said insulating layer prior to forming said first etched region wherein said hard mask layer comprises silicon nitride.

9. A method of forming a dual damascene interconnect in an integrated circuit comprising:

providing a substrate having a first etched region therein;

filling said first etched region with a bottom antireflective coating (BARC) layer;

coating said BARC layer with a resist layer;

patterning said resist layer and said BARC layer to define an opening encompassing said first etched opening wherein said BARC layer is recessed within said first etched opening;

thereafter forming a second etched region encompassing a top portion of said first etched region;

thereafter removing said resist layer and said BARC layer; and

thereafter filling said first and second etched regions with a conductive material to complete formation of said interconnect.

10. The method according to Claim 9 wherein said BARC material has the following properties:

it absorbs light at a wavelength used to expose said resist;

it completely fills said first etched region; and

it can be partially removed by a developer used to remove said resist.

11. The method according to Claim 9 wherein said BARC material comprises polyimide or organic type ARC material.

12. The method according to Claim 9 wherein said first etched region forms a via hole and wherein said second etched region forms a trench and wherein said via hole and said trench together form a dual damascene opening.

13. The method according to claim 9 wherein the said BARC layer recessed within said first etched region has a height of between about 50% and 95% of a height of said first etched region.

14. The method according to Claim 9 wherein said first and second etched region are etched through an insulating layer comprising silicon dioxide or low dielectric constant dielectric materials.

15. The method according to Claim 14 further comprising depositing a hard mask layer overlying said insulating layer prior to forming said first etched region wherein said hard mask layer comprises silicon nitride.

16. A method of forming an integrated circuit having a dual damascene interconnect structure comprising:

providing a substrate having a first etched region therein;

filling said first etched region with a first protective layer;

etching back said first protective layer to form a recessed plug within said first etched opening;

coating said substrate and said recessed plug with a second protective layer;

coating said second protective layer with a resist layer;

patterning said resist layer and said second protective layer to define an opening encompassing said first etched opening wherein said second protective layer within said opening is removed and wherein said first protective layer remains within said first etched opening;

thereafter forming a second etched region encompassing a top portion of said first etched region;

thereafter removing said resist layer and said first and second protective layers; and

thereafter filling said first and second etched regions with a conductive material to complete formation of said dual damascene interconnect.

17. The method according to Claim 16 wherein said first protective layer is a BARC material having a high etch rate.

18. The method according to claim 17 wherein said high etch rate BARC material has the following properties:

it may be etched at least 25 % or more faster than layers through which said first and second etched openings are made;

it completely fills said first etched region; and

it absorbs light at a wavelength used to expose said resist.

19. The method according to claim 17 wherein said high etch rate BARC material comprises polyimide or organic type ARC material.

20. The method according to Claim 16 wherein said first protective layer is a resin.

21. The method according to Claim 16 wherein said second protective layer is a BARC material.

22. The method according to claim 21 wherein said BARC material has the following properties:

it absorbs light at a wavelength used to expose said resist;

it completely fills said first etched region; and

it may be partially removed by a developer used to remove said resist.

23. The method according to claim 21 wherein said BARC material comprises polyimide or organic type ARC material.